

LADDER ANALYSIS PROGRAM

FOR THE HP-41C



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"BLAP": BACKWARDS LADDER ANALYSIS PROGRAM
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ONE OF THE SIMPLEST WAYS TO ANALYZE A LADDER CIRCUIT IS TO ASSUME AN OUTPUT CURRENT; THEN WORK BACKWARDS THROUGH THE NETWORK OBTAINING ALL VOLTAGES AND CURRENTS IN TERMS OF THE ASSUMED OUTPUT CURRENT. FOR A LINEAR NETWORK, GAIN AND IMPEDANCE THROUGHOUT THE CIRCUIT ARE INDEPENDENT OF ACTUAL CURRENT AND VOLTAGE LEVELS AND THE RESPONSE (ALL VOLTAGES AND CURRENTS) DUE TO ONE VALUE OF EXCITATION MAY BE LINEARLY SCALED TO ANOTHER VALUE OF EXCITATION - FOR EXAMPLE YOU MIGHT WANT TO KNOW ALL VOLTAGES AND CURRENTS WITHIN A CIRCUIT FOR A SPECIFIC INPUT POWER IN ORDER TO DETERMINE THE VOLTAGE AND CURRENT RATINGS OF ALL THE COMPONENTS.

"BLAP" IS A COLLECTION OF SUBROUTINES FOR THE HP-41C WHICH EMPLOYS THE "BACKWARDS" ALGORITHM. THE LOAD CURRENT IS ASSUMED $1.0 + j0$ AMPERES FOR CONVENIENCE. THIS MAKES THE LOAD VOLTAGE R_L VOLTS FOR RESISTIVE LOAD R_L AND THE LOAD POWER IS R_L WATTS. WORKING BACK TOWARD THE GENERATOR; IF A SERIES IMPEDANCE IS ENCOUNTERED THE CURRENT IS UNCHANGED BUT THE VOLTAGE IS INCREASED BY THE DROP ACROSS THE SERIES IMPEDANCE ($V = V + I * Z_S$). IF A PARALLEL ADMITTANCE IS ENCOUNTERED THE VOLTAGE IS UNCHANGED BUT THE CURRENT IS INCREASED BY THE CURRENT FLOWING THROUGH THE SHUNT ADMITTANCE ($I = I + Y_P * V$). A LIBRARY OF 28 SERIES/PARALLEL TYPE ELEMENTS IS AVAILABLE (ALL SIMPLE SERIES/PARALLEL RLC COMBINATIONS, OPEN AND SHORTED TRANSMISSION LINE STUBS, AND SERIES AND SHUNT IMPEDANCES). TWO-PORT ELEMENTS MAY ALSO BE INCLUDED IN A LADDER CIRCUIT. FOUR TWO-PORT ELEMENTS ARE PROVIDED:

GB RESISTIVE FEEDBACK GAIN BLOCK
BG "BACKWARDS" GAIN BLOCK
TL TRANSMISSION LINE
TF IDEAL TRANSFORMER.

THE GAIN BLOCK IS A REASONABLE APPROXIMATION OF A SINGLE TRANSISTOR BROADBAND RESISTIVE FEEDBACK AMPLIFIER WHICH IS COMMONLY EMPLOYED IN MODERN CIRCUIT DESIGN (AVANTEK, OPTIMAX, W-J, ANZAC, ETC. AMPLIFIERS) AND INCLUDES THE COUPLING FROM LOAD TO SOURCE DUE TO THE INTENTIONAL FEEDBACK. BG IS THE SAME GAIN BLOCK IN THE REVERSE DIRECTION WHICH ALLOWS ANALYSIS IN EITHER DIRECTION OF ANY LADDER CIRCUIT, EVEN ONE INCLUDING AMPLIFIERS.

ALL ELEMENT SUBROUTINES ARE GIVEN GLOBAL LABELS SO THAT THEY MAY BE CALLED BY A SEPARATE PROGRAM WHICH DESCRIBES THE CIRCUIT. OTHER ELEMENT SUBROUTINES MAY BE ADDED TO "BLAP" -OR UNUSED ONES MAY BE DELETED. THE SUBROUTINE MUST COMPUTE THE INPUT CURRENT AND VOLTAGE IN TERMS OF THE "KNOWN" OUTPUT CURRENT AND VOLTAGE FOR THE ELEMENT BEING MODELED. A BRIEF STUDY OF THE REGISTER USAGE, THE APPENDIX, AND THE PROGRAM LISTING OF SOME OF THE SUBROUTINES USED SHOULD ENABLE THE USER TO GENERATE HIS OWN NEW ELEMENTS.

SIX "COMPUTE AND PRINT" COMMANDS ARE AVAILABLE IN THE BLAP PROGRAM:

- "RL" INITIALIZES LOAD AND "AVIEWS" FREQUENCY
- "RG" COMPUTES AND "AVIEWS" GAIN
- "S" COMPUTES AND "AVIEWS" FORWARD AND INPUT "S" PARAMETERS (SF AND SI) IN DB
- "Z" COMPUTES AND "AVIEWS" $Z=V/I$ AT ANY POINT
- "VP" "AVIEWS" V AT ANY POINT
- "IS" "AVIEWS" I AT ANY POINT

EXCEPT FOR "RL" WHICH INITIALIZES THE CIRCUIT (AND IS THE FIRST COMMAND USUALLY EXECUTED), THE V,I DATA IS NOT DISTURBED BY ANY OF THE COMMANDS SO THESE MAY BE EXECUTED ANYWHERE WITHIN THE CIRCUIT. "RG" OR "S" WILL NORMALLY BE THE LAST COMMAND EXECUTED. IN ADDITION TO THE SIX COMMANDS ABOVE, REGISTER USAGE IN BLAP IS COMPATIBLE WITH "PRPLOT" IN THE PRINTER ROM MAKING IT EASY TO PLOT ANY DESIRED CIRCUIT RESPONSE. "PRPLOT" SUPPLIES THE FREQUENCY TO THE CIRCUIT DESCRIPTION PROGRAM WHICH IN TURN RETURNS THE COMPUTED PARAMETER TO "PRPLOT".

USING BLAP

"BLAP" COMMANDS MAY BE MANUALLY EXECUTED TO ANALYZE A GIVEN CIRCUIT AT A SINGLE FREQUENCY; HOWEVER MOST OF THE TIME THE COMMANDS WILL BE STORED IN A PROGRAM IN ORDER TO "SWEEP" THE SELECTED RESPONSE VERSUS FREQUENCY. THE PRESENT ANALYSIS FREQUENCY -IN GHZ- MUST BE STORED IN REGISTER 08 SO THE CIRCUIT DESCRIPTION PROGRAM WILL USUALLY BE CONTAINED WITHIN A LOOP WHICH INCREMENTS R08 EITHER LINEARLY (ADDITIVE INCREMENTS) OR LOGARITHMICALLY (MULTIPLICATIVE INCREMENTS). "PRPLOT" AUTOMATICALLY PROVIDES A LINEARLY INCREMENTED FREQUENCY (X) LOOP. "PRPLOT" CAN BE MADE TO PROVIDE MULTIPLICATIVE INCREMENTS BY INITIALLY SPECIFYING A SMALL NON ZERO "X INCREMENT" THEN MULTIPLY R06 BY THE DESIRED INCREMENT IN THE CIRCUIT DESCRIPTION PROGRAM (R06 IS "PRPLOT" X). R17 CONTENTS ARE TACKED ONTO THE DISPLAY NAME FOR "Z", "VP", OR "IS" TO KEEP TRACK OF THE OUTPUT DATA. USUALLY START WITH 0 IN R17 AT LOAD END AND INCREMENT R17 BY ONE FOR EACH NEW ELEMENT ADDED. BEGIN THE PROGRAM WITH AN "RL" LOAD INITIALIZE COMMAND THEN WORK TOWARD THE GENERATOR USING THE ELEMENT COMMANDS TO DESCRIBE THE CIRCUIT - YOU MAY ASSIGN OFTEN-USED COMMANDS AND ELEMENTS TO USER KEYS TO SAVE TIME. OUTPUT COMMANDS MAY BE INSERTED ANYWHERE INTERMEDIATE RESULTS ARE DESIRED. THE LAST COMMAND WITHIN THE CIRCUIT DESCRIPTION LOOP WILL NORMALLY BE EITHER "RG" OR "S" TO OBTAIN THE OVERALL RESPONSE. EXAMPLES OF "BLAP" INCLUDING USING THE PLOTTER AND BOTH LINEAR AND LOG FREQUENCY SCALES ARE INCLUDED ALONG WITH THE PROGRAM LISTING TO AID THE USER IN CREATING HIS OWN CIRCUIT DESCRIPTION PROGRAMS.

COMPLEX NUMBER MATHEMATICS IS USUALLY REQUIRED FOR CIRCUIT ANALYSIS (EXCEPT AT DC OR FOR RESISTORS ONLY). "BLAP" CARRIES COMPLEX NUMBERS IN RECTANGULAR FORM FOR ALL OPERATIONS IN ORDER TO ACHIEVE A SPEED IMPROVEMENT OVER USING R-P AND P-R OPERATIONS. THE ROUTINES WITHIN "BLAP" EMPLOY ONLY STACK REGISTERS (X,Y,Z,T,L), R04, AND FLAG 14. "+" AND "-" EVEN SAVE "LAST X+JY" IN THE STACK (Z+JT). THE COMPLEX ARITHMETIC COMMANDS MAY BE EMPLOYED FOR GENERAL USE OUTSIDE OF "BLAP" - JUST REMEMBER THAT "1" USES REGISTER 04; ALL OTHER COMPLEX OPERATIONS AFFECT ONLY THE STACK.

QUICK REFERENCE GUIDE

>AT LEAST TWO MEMORY MODULES ARE REQUIRED<

BLAP COMMANDS:

| NAME | DATA FORMAT | FUNCTION PERFORMED |
|------|-------------|-----------------------------|
| RL | RL | INITIALIZE LOAD RESISTANCE |
| RG | RG | COMPUTE GAIN FOR RG GEN. |
| S | RG | COMPUTE SF AND SI FOR RL/RG |
| Z | (USE R17 | COMPUTE IMPEDANCE |
| VP | A5 INDEX | COMPUTE VOLTAGE TO GROUND |
| IS | MARKER) | COMPUTE SERIES CURRENT |

BLAP ELEMENTS:

| NAME | DATA FORMAT | FUNCTION PERFORMED |
|------|------------------|--------------------------|
| BG | R0 ↗ GDB | REVERSE GAIN BLOCK |
| GB | R0 ↗ GDB | TRANSISTOR GAIN BLOCK |
| TL | R0 ↗ θ0 ↗ F0 | TRANSMISSION LINE |
| TF | N1 ↗ N2 | IDEAL TRANSFORMER |
| PRXS | R ↗ L ↗ C | PARALLEL RLC IN SERIES |
| PRXP | R ↗ L ↗ C | PARALLEL RLC IN PARALLEL |
| SRXP | R ↗ L ↗ C | SERIES RLC IN PARALLEL |
| SRXS | R ↗ L ↗ C | SERIES RLC IN SERIES |
| PLCS | L ↗ C | PARALLEL LC IN SERIES |
| PLCP | L ↗ C | PARALLEL LC IN PARALLEL |
| SLCP | L ↗ C | SERIES LC IN PARALLEL |
| SLCS | L ↗ C | SERIES LC IN SERIES |
| PROS | R ↗ C | PARALLEL RC IN SERIES |
| PROP | R ↗ C | PARALLEL RC IN PARALLEL |
| SROF | R ↗ C | SERIES RC IN PARALLEL |
| SROS | R ↗ C | SERIES RC IN SERIES |
| PRLS | R ↗ L | PARALLEL RL IN SERIES |
| PRLP | R ↗ L | PARALLEL RL IN PARALLEL |
| SRLP | R ↗ L | SERIES RL IN PARALLEL |
| SRLS | R ↗ L | SERIES RL IN SERIES |
| RP | R OHMS | R IN PARALLEL |
| RS | R | R IN SERIES |
| LP | L N _h | L IN PARALLEL |
| LS | L | L IN SERIES |
| CP | C PF | C IN PARALLEL |
| CS | C | C IN SERIES |
| ZP | R ↗ X | R+JX IN PARALLEL |
| ZS | R ↗ X | R+JX IN SERIES |
| OSTP | R0 ↗ θ0 ↗ F0 | OPEN STUB IN PARALLEL |
| OSTS | R0 ↗ θ0 ↗ F0 | OPEN STUB IN SERIES |
| SSTP | R0 ↗ θ0 ↗ F0 | SHORTED STUB IN PARALLEL |
| SSTS | R0 ↗ θ0 ↗ F0 | SHORTED STUB IN SERIES |

| COMPLEX MATH OPERATOR | | OPERATION PERFORMED |
|-----------------------|---|----------------------|
| | 1 | $X+JY=1/(X+JY)$ |
| | / | $X+JY=(Z+JT)/(X+JY)$ |
| | * | $X+JY=(X+JY)*(Z+JT)$ |
| < "LAST X+JY" > | + | $X+JY=(X+JY)+(Z+JT)$ |
| < SAVED IN Z+JT > | - | $X+JY=(Z+JT)-(X+JY)$ |

REGISTER USE:(MIN SIZE 020, DEG MODE, F00-04 CLEAR)

| | | | |
|-----|-------------------|-----|------------------|
| 00 | PLOTTER YMAX | 10 | PLOTTER XINC |
| 01 | PLOTTER YMIN | 11 | PLOT "NAME" |
| 02 | PLOT NNN.AAA | >12 | RE(V) |
| 03 | PLOT CHARACTER | >13 | IM(V) |
| <04 | SCRATCH REGISTER | >14 | RE(I) |
| 05 | PLOTTER "FIX" N | >15 | IM(I) |
| 06 | PLOTTER FREQUENCY | >16 | RL |
| 07 | PLOTTER "X UNITS" | >17 | INDEX SYMBOL |
| <08 | FREQUENCY GHZ | >18 | SCRATCH REGISTER |
| 09 | PLOTTER XMAX | >19 | SCRATCH REGISTER |

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| | | |
|----------------|----------------|----------------|
| 001>LBL "BLAP" | 061>LBL 01 | 121 SF 04 |
| 002 PFC 3948 | 062 RCL 15 | 122>LBL "SRXP" |
| 003 PROMPT | 063 RCL 04 | 123 SF 00 |
| 004>LBL "RL" | 064 * | 124>LBL "SRXS" |
| 005 STO 16 | 065 ST+ 13 | 125>LBL 00 |
| 006 STO 12 | 066 RDN | 126 SF01 |
| 007 1 | 067 RCL 14 | 127 GTO 00 |
| 008 STO 14 | 068 RCL 04 | 128>LBL "PLCS" |
| 009 0 | 069 * | 129 SF 04 |
| 010 STO 13 | 070 ST+ 12 | 130 GTO 00 |
| 011 STO 15 | 071 RDN | 131>LBL "PLCP" |
| 012 FIX 3 | 072 GTO 05 | 132 SF 04 |
| 013 "F=" | 073>LBL "TL" | 133>LBL "SLCP" |
| 014 ARCL 08 | 074 / | 134 SF00 |
| 015 "H Gnz" | 075 RCL 08 | 135>LBL "SLCS" |
| 016 AVIEW | 076 * | 136>LBL 00 |
| 017 FIX 2 | 077 1 | 137 SF 03 |
| 018 RTN | 078 F-R | 138 SF 02 |
| 019>LBL "BG" | 079 RDN | 139 GTO 07 |
| 020 SF 00 | 080 STO 04 | 140>LBL "PRCS" |
| 021>LBL "GB" | 081 X<>Y | 141 SF 04 |
| 022 Z0 | 082 ST/ 04 | 142 GTO 00 |
| 023 / | 083 * | 143>LBL "PRCP" |
| 024 10↗ X | 084 STO L | 144 SF 04 |
| 025 Z | 085 R↗ | 145>LBL "SRCP" |
| 026 / | 086 RCL 13 | 146 SF 00 |
| 027 ENTER↗ | 087 RCL 12 | 147>LBL "SRCS" |
| 028 X↗ 2 | 088 RCL 15 | 148>LBL 00 |
| 029 LAST X | 089 R↗ | 149 ENTER↗ |
| 030 ST+ X | 090 ST* 12 | 150 SF 01 |
| 031 + | 091 ST* 13 | 151 SF 03 |
| 032 1 | 092 ST* 15 | 152 GTO 07 |
| 033 + | 093 X<> 14 | 153>LBL "PRLS" |
| 034 SQRT | 094 ST* 14 | 154 SF 04 |
| 035 + | 095 X<> L | 155 GTO 00 |
| 036 ST/ Z | 096 ST* L | 156>LBL "PRLP" |
| 037 ST/ T | 097 ST* Y | 157 SF 04 |
| 038 * | 098 RDN | 158>LBL "SRLP" |
| 039 STO 04 | 099 ST- 12 | 159 SF 00 |
| 040 FC?C 00 | 100 RDN | 160>LBL "SRLS" |
| 041 GTO 00 | 101 LAST X | 161>LBL 00 |
| 042 RCL 13 | 102 ST+ 13 | 162 ENTER↗ |
| 043 RCL 12 | 103 RDN | 163 SF 01 |
| 044 R↗ | 104 RCL 04 | 164 SF 02 |
| 045 ST/ Z | 105 ST* Z | 165 GTO 07 |
| 046 / | 106 * | 166>LBL "RF" |
| 047 GTO 01 | 107 X<>Y | 167 SF 00 |
| 048>LBL 00 | 108 CHS | 168>LBL "RS" |
| 049 - | 109 GTO 05 | 169 ENTER↗ |
| 050 ST/ 12 | 110>LBL "TF" | 170 ENTER↗ |
| 051 ST/ 13 | 111 / | 171 SF 01 |
| 052 / | 112 ST* 12 | 172 GTO 07 |
| 053 ST* 14 | 113 ST* 13 | 173>LBL "LP" |
| 054 ST* 15 | 114 ST/ 14 | 174 SF 00 |
| 055 RCL 13 | 115 ST/ 15 | 175 LBL "LS" |
| 056 RCL 12 | 116 RTN | 176 ENTER↗ |
| 057 R↗ | 117>LBL "PRXS" | 177 SF 02 |
| 058 ST* 12 | 118 SF 04 | 178 GTO 07 |
| 059 ST* 13 | 119 GTO 03 | 179>LBL "CP" |
| 060 RDN | 120>LBL "PRXP" | 180 SF 00 |

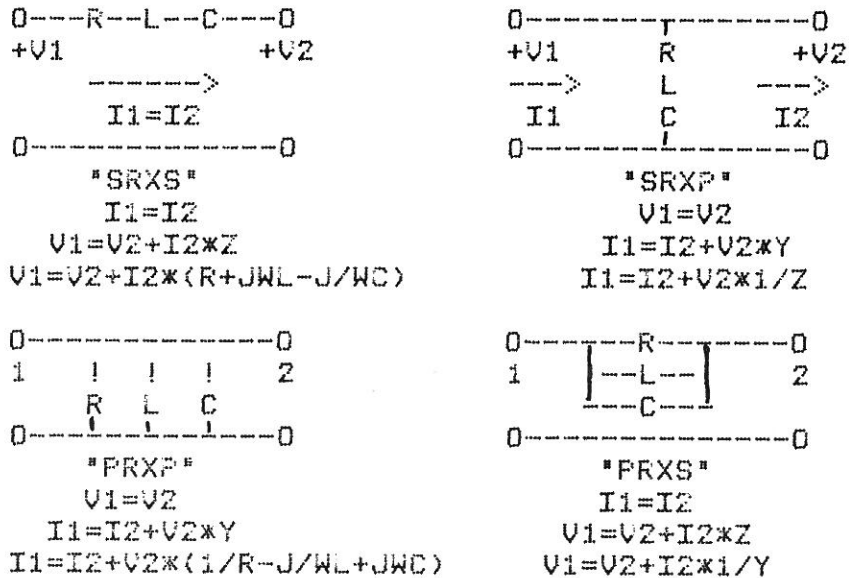
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|----------------|--------------|--------------|
| 181>LBL "CS" | 241 * | 301 RCL 19 |
| 182 SF 03 | 242 0 | 302 RCL 18 |
| 183>LBL 07 | 243>LEL 00 | 303 XEQ "—" |
| 184 STO 04 | 244 FS?C 00 | 304 RDN |
| 185 RDN | 245 GTD 00 | 305 RDN |
| 186 PI | 246 FS?C 04 | 306 XEQ "/" |
| 187 ST+ X | 247 XEQ "1" | 307 "SI" |
| 188 RCL 08 | 248 RCL 15 | 308>LBL 00 |
| 189 * | 249 RCL 14 | 309 "FDB" |
| 190 * | 250 XEQ "*" | 310 R-P |
| 191 LAST X | 251 ST+ 12 | 311 LOG |
| 192 -1 E3 | 252 RDN | 312 20 |
| 193 / | 253 ST+ 13 | 313 * |
| 194 RCL 04 | 254 RTN | 314 GTD 01 |
| 195 * | 255>LBL 00 | 315>LBL "Z" |
| 196 FC?C 03 | 256 FC?C 04 | 316 RCL 13 |
| 197 CLX | 257 XEQ "1" | 317 RCL 12 |
| 198 X#0? | 258 RCL 13 | 318 RCL 15 |
| 199 1/X | 259 RCL 12 | 319 RCL 14 |
| 200 XEQ 01 | 260 XEQ "*" | 320 XEQ "/" |
| 201 X<>Y | 261>LBL 05 | 321 "Z" |
| 202 FC?C 02 | 262 ST+ 14 | 322 GTD 00 |
| 203 CLX | 263 RDN | 323>LBL "VP" |
| 204 XEQ 01 | 264 ST+ 15 | 324 RCL 13 |
| 205 + | 265 RTN | 325 RCL 12 |
| 206 X<>Y | 266>LBL "S" | 326 "V" |
| 207 FC?C 01 | 267 SF 00 | 327 GTD 00 |
| 208 CLX | 268>LBL "RG" | 328>LBL "IS" |
| 209 XEQ 01 | 269 STO 04 | 329 RCL 15 |
| 210 FS? 04 | 270 RCL 15 | 330 RCL 14 |
| 211 CHS | 271 RCL 14 | 331 "I" |
| 212 GTD 00 | 272 RCL 04 | 332>LBL 00 |
| 213>LBL 01 | 273 ST* Z | 333 FIX 0 |
| 214 FC? 04 | 274 * | 334 CF 29 |
| 215 RTN | 275 RCL 13 | 335 ARCL 17 |
| 216 X#0? | 276 RCL 12 | 336 FIX 2 |
| 217 1/X | 277 XEQ "+" | 337 SF 29 |
| 218 CHS | 278 STO 16 | 338 R-P |
| 219 RTN | 279 X<>Y | 339>LBL 01 |
| 220>LBL "ZF" | 280 STO 19 | 340 RND |
| 221 SF 00 | 281 X<>Y | 341 X<>Y |
| 222>LBL "ZS" | 282 RCL 04 | 342 RND |
| 223 X<>Y | 283 RCL 16 | 343 X<>Y |
| 224 GTD 00 | 284 * | 344 "t=" |
| 225>LBL "OSTP" | 285 SQRT | 345 ARCL X |
| 226 SF 00 | 286 ST+ X | 346 "t<" |
| 227>LBL "OSTS" | 287 ST/ Z | 347 ARCL Y |
| 228 SF 04 | 288 / | 348 AVIEW |
| 229 GTD 01 | 289 XEQ "1" | 349 RTN |
| 230>LBL "SSTP" | 290 "G" | 350>LBL "/" |
| 231 SF 00 | 291 FS? 00 | 351 SF 14 |
| 232>LBL "SSTS" | 292 "SF" | 352>LBL "1" |
| 233>LEL 01 | 293 XEQ 00 | 353 STO 04 |
| 234 / | 294 FC?C 00 | 354 X↗ 2 |
| 235 RCL 08 | 295 RTN | 355 RDN |
| 236 * | 296 RCL 13 | 356 CHS |
| 237 TAN | 297 RCL 12 | 357 X↗ 2 |
| 238 X<>Y | 298 2 | 358 ST+ T |
| 239 FS? 04 | 299 ST* Z | 359 X↙L |
| 240 1/X | 300 * | 360 R↗ |

361 ST/ 04
362 /
363 RCL 04
364 FCFC 14
365 RTN
366>LBL "x"
367 STD L
368 R↗
369 ST* L
370 R↗
371 ST* Z
372 R↗
373 ST* Z
374 ST* Y
375 X↔L
376 +
377 X↔T
378 RDN
379 -
380 RTN
381>LBL "+"
382 ST+ Z
383 RDN
384 ST+Z
385 RDN
386 RTN
387>LBL "-"
388 ST- Z
389 RDN
390 ST- Z
391 RDN
392 END 844 BYTES

APPENDIX

THE DERIVATION OF SOME OF THE "BLAP" ELEMENT SUBROUTINES IS PRESENTED IN THIS SECTION TO AID THE USER IN CREATING CUSTOMIZED SUBROUTINES FOR HIS NEEDS. FAMILIARITY WITH CIRCUIT ANALYSIS AND WITH USING THE HF-41C ARE THE ONLY PREREQUISITES.

SERIES-PARALLEL RLC'S



EITHER THE IMPEDANCE OF A SERIES RLC OR THE ADMITTANCE OF A PARALLEL RLC IS COMPUTED. "Z<>Y" TRANSFORMATION -IF NECESSARY- IS PERFORMED USING THE "1" COMMAND. FLAG 04 IS USED TO DISTINGUISH BETWEEN SERIES OR PARALLEL RLC CONNECTION WITHIN THE ELEMENT -F04 IS SET IF THE FIRST LETTER OF THE "NAME" IS "P" -. FLAG 00 IS USED TO DISTINGUISH BETWEEN SERIES OR PARALLEL USAGE OF THE ELEMENT WITHIN THE LADDER NETWORK -F00 IS SET IF THE LAST LETTER OF THE ELEMENT "NAME" IS "P" -. F01, F02, AND F03 ARE SET IF RESPECTIVELY R, L, OR C ARE PRESENT WITHIN THE BLOCK. THE FLAGS ARE TESTED LATER TO REMOVE ANY UNUSED ELEMENTS FROM THE GENERAL RLC ELEMENT. IF FLAGS 00 AND 04 MATCH, THE ELEMENT IS USED AS IS, OTHERWISE THE "1" COMMAND CONVERTS Z<>Y.

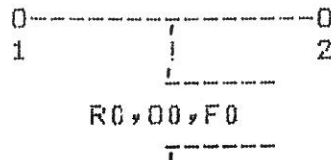
STUBS

TRANSMISSION LINE STUBS MAY ALSO SIMPLY BE REPRESENTED AS IMPEDANCES OR ADMITTANCES. THE SHORTED STUB IS REPRESENTED AS AN IMPEDANCE, WHILE THE OPEN STUB IS REPRESENTED AS AN ADMITTANCE.



$$R_0 = 00, F_0$$

"SSTS"
 $I_1 = I_2$
 $V_1 = V_2 + I_2 * Z$
 $Z = 0 + jR_0 * TAND$
 $O = 00 * F / F_0$



$$R_0 = 00, F_0$$

"OSTP"
 $V_1 = V_2$
 $I_1 = I_2 + V_2 * Y$
 $Y = 0 + j(1/R_0) * TAND$
 $O = 00 * F / F_0$

THE ONLY DIFFERENCE BETWEEN THE SHORTED STUB IMPEDANCE -Z- AND THE OPEN STUB ADMITTANCE -Y- IS R_0 VERSUS $1/R_0$. FLAG 04 IS SET FOR AN OPEN STUB -FIRST LETTER "O" AND FLAG 00 IS SET FOR PARALLEL STUB USAGE - LAST LETTER "P". ONCE THE STUB IMPEDANCE OR ADMITTANCE IS DETERMINED THE ELEMENT IS HANDED WITHIN "BLAP" JUST LIKE A LUMPED IMPEDANCE OR ADMITTANCE.

ALMOST ANY PASSIVE FILTER MAY BE ANALYZED USING ONLY THE IMPEDANCE/ADMITTANCE ELEMENTS DESCRIBED ABOVE. "BLAP" DOES NOT PROVIDE ALL POSSIBLE RLC COMBINATIONS; HOWEVER, AND ALSO THE USER MIGHT FIND IT CONVENIENT AND FASTER TO CREATE COMBINATIONS OF EXISTING ELEMENTS. TWO EXAMPLES WHICH MIGHT WARRANT THEIR OWN COMMANDS ARE A QUARTZ CRYSTAL -SERIES RLC WITH A CAPACITOR IN PARALLEL- AND A REAL COIL OR RESISTOR -SERIES RL IN PARALLEL WITH A CAPACITOR. THESE ELEMENTS MAY BE REALIZED USING NORMAL "BLAP" COMMANDS ONLY IF THEY ARE USED AS PARALLEL ELEMENTS.

TWO-PORT ELEMENTS

ALL OF THE ELEMENTS DESCRIBED SO FAR HAVE EITHER IDENTICAL VOLTAGE ON EITHER SIDE -PARALLEL ELEMENT- OR IDENTICAL CURRENT ON EITHER SIDE -SERIES ELEMENT. MANY VERY USEFUL ELEMENTS MODIFY BOTH THE CURRENT AND VOLTAGE AND MUST BE CONSIDERED AS TWO-PORT NETWORKS -IN FACT THE ELEMENTS DESCRIBED ABOVE ARE SPECIAL TRIVIAL CASES OF TWO-PORT NETWORKS-. THE INPUT/OUTPUT RELATIONSHIP OF A TWO-PORT CAN BE DESCRIBED IN MANY EQUIVALENT WAYS - $Z, Y, G, H, S, ABCD$ - DEPENDING UPON THE CHOICE FROM I_1, V_1, I_2, V_2 OF THE PAIRS OF INDEPENDENT AND DEPENDENT VARIABLE PAIRS. IN "BLAP" I_2 , AND V_2 ARE THE INDEPENDENT VARIABLES SO WE ARE REALLY USING "BACKWARDS" ABCD PARAMETERS. THE FOUR TWO-PORTS USED IN "BLAP" ARE PRESENTED BELOW:

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0-----0
+V1 R0,G0,F0 +V2
I1-->      -->I2
0-----0

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"TL"

```

I1=I2*COSG0+JV2*(1/R0)*SINO
V1=V2*COSG0+JI2*R0*SINO
O=00*F/F0

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0-----0
+V1 N1:N2 +V2
I1-->      -->I2
0-----0

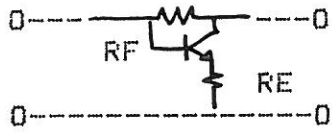
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"TF"

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I1=I2*N2/N1
V1=V2*N1/N2
N1, N2 +/-

```



"GB"

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(RE*RF*I2+RE*V2)
V1=-----
RE-RF

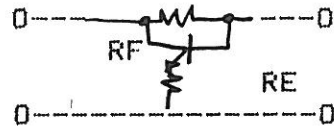
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(RE*I2+V2)

```

I1=-----
RE-RF

```



"BG"

```

V1=RF*I2+V2
I1=I2+V2/RE

```

R0=SQRT(RF*RE)

S21=(RE-RF)/(RE+R0)

GDB=20*LOG(S21)

THE TWO-PORTS INCLUDED ARE ALL "IDEAL" ELEMENTS. THE TRANSMISSION LINE AND TRANSFORMER ARE LOSSLESS AND THE GAIN BLOCK IS BUILT USING AN IDEAL TRANSISTOR SUCH THAT THE AMPLIFIER PERFORMANCE IS SOLELY DETERMINED BY THE FEEDBACK RESISTORS. THE GAIN BLOCK HAS 180 DEGREES PHASE SHIFT AND IS A PERFECT MATCH IN A R0 OHM SYSTEM. "BLAP" ACTUALLY "DESIGNS" EACH GAIN BLOCK - COMPUTES RF AND RE FOR SPECIFIED DB GAIN AND SYSTEM RESISTANCE R0-. SIMULTANEOUS PERFECT MATCH WITH THE GAIN BLOCK IS ONLY POSSIBLE IF THE GENERATOR AND LOAD IMPEDANCES ARE EQUAL. THE "GB" MAY ALWAYS BE CASCADED WITH A TRANSFORMER OR MATCHING NETWORK TO OBTAIN ANY COMBINATION OF SOURCE AND LOAD IMPEDANCES. THE GAIN BLOCK IS UNCONDITIONALLY STABLE SINCE THE INPUT AND OUTPUT MATCH IS PERFECT IN A R0 OHM SYSTEM AND THE REVERSE ISOLATION IS GREATER THAN THE FORWARD GAIN.

CANDIDATES FOR OTHER TWO-PORT ELEMENTS ARE LIMITLESS. LOSSY TRANSMISSION LINE, NON-IDEAL TRANSFORMERS, AND GAIN BLOCKS HAVING "REAL" TRANSISTORS ARE OBEVIOUS EXAMPLES. HAPPY PROGRAMMING!

